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National Semiconductor

February 1988

CD4023BM/CD4023BC
Buffered Triple 3-Input NAND Gate
CD4025BM/CD4025BC
Buffered Triple 3-Input NOR Gate

CD4023BM/CD4023BC Buffered Triple 3-Input NAND Gate
CD4025BM/CD4025BC Buffered Triple 3-Input NOR Gate

General Description

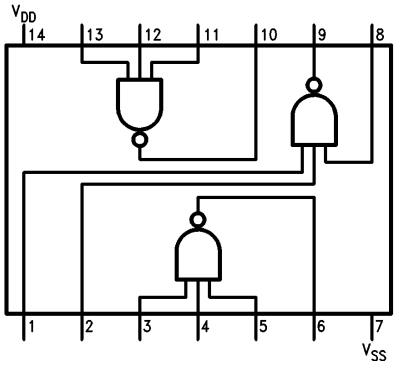
These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

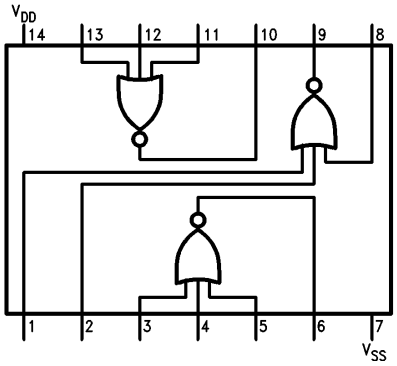
CD4023BM/CD4023BC
Dual-In-Line Package



TL/F/5956–1

Top View

CD4025BM/CD4025BC
Dual-In-Line Package



TL/F/5956–2

Top View

Order Number CD4023B or CD4025B

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD}+0.5\ V_{DC}$
Storage Temp. Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

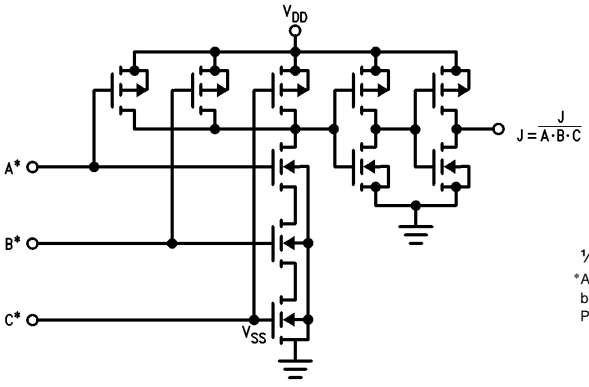
DC Supply Voltage (V_{DD})	$5\ V_{DC}$ to $15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4023BM, CD4025BM	$-55°C$ to $+125°C$
CD4023BC, CD4025BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4023BM, CD4025BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Typ	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$		0.5		0.005	0.5		15	μA
		$V_{DD} = 15V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V, V_O=4.5V$ } $\lvert I_O\rvert<1\mu A$		1.5		2	1.5		1.5	V
		$V_{DD}=10V, V_O=9.0V$ } $\lvert I_O\rvert<1\mu A$		3.0		4	3.0		3.0	V
		$V_{DD}=15V, V_O=13.5V$ } $\lvert I_O\rvert<1\mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ } $\lvert I_O\rvert<1\mu A$	3.5		3.5	3		3.5		V
		$V_{DD}=10V, V_O=1.0V$ } $\lvert I_O\rvert<1\mu A$	7.0		7.0	6		7.0		V
		$V_{DD}=15V, V_O=1.5V$ } $\lvert I_O\rvert<1\mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Schematic Diagram

CD4023BC/CD4023BM



⅓ Device Shown

*All Inputs Protected by Standard CMOS Input Protection Circuit.

TL/F/5956–3

DC Electrical Characteristics CD4023BC, CD4025BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Typ	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.004	1.0		7.5	μA
		V_{DD} = 10V		2.0		0.005	2.0		15	μA
		V_{DD} = 15V		4.0		0.006	4.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V, $\lvert I_O \rvert < 1\mu A$		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V, $\lvert I_O \rvert < 1\mu A$		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V, $\lvert I_O \rvert < 1\mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V, $\lvert I_O \rvert < 1\mu A$	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V, $\lvert I_O \rvert < 1\mu A$	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V, $\lvert I_O \rvert < 1\mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

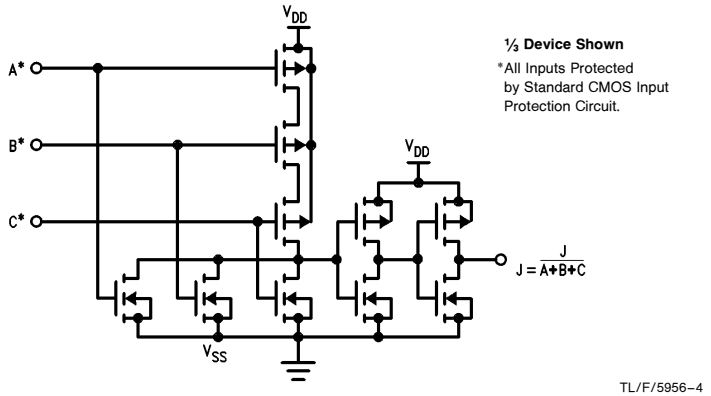
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Schematic Diagram

CD4025BM/CD4025BC



TL/F/5956–4

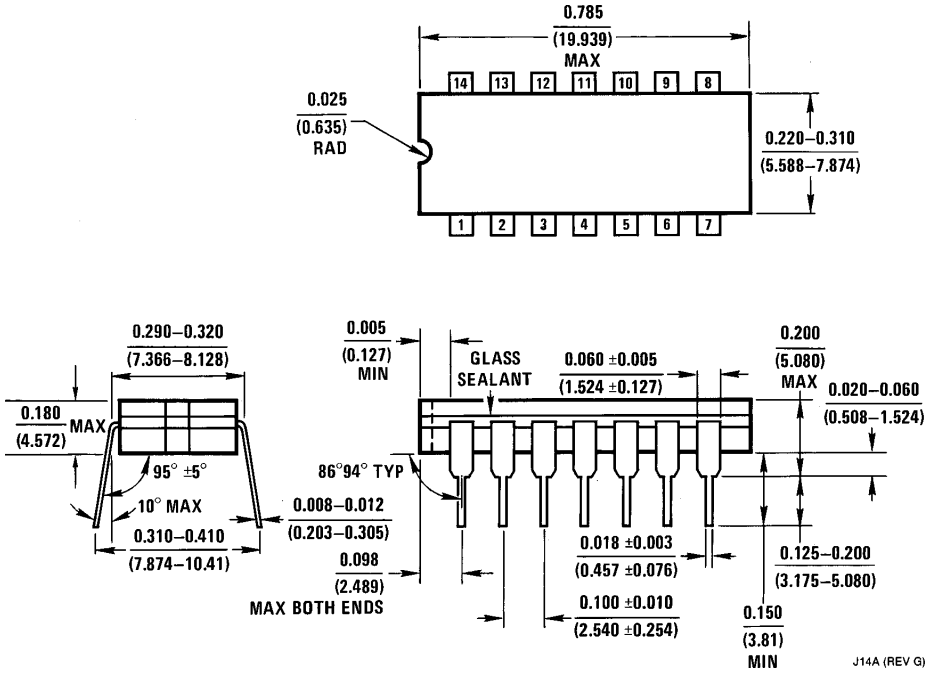
AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, unless otherwise specified

Symbol	Parameter	Conditions	CD4023BC CD4023BM			CD4025BC CD4025BM			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PHL}	Propagation Delay, High-to-Low Level	$V_{DD} = 5V$		130	250		130	250	ns
		$V_{DD} = 10V$		60	100		60	100	ns
		$V_{DD} = 15V$		40	70		40	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	$V_{DD} = 5V$		110	250		120	250	ns
		$V_{DD} = 10V$		50	100		60	100	ns
		$V_{DD} = 15V$		35	70		40	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		90	200		90	200	ns
		$V_{DD} = 10V$		50	100		50	100	ns
		$V_{DD} = 15V$		40	80		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 4)	Any Gate		17			17		pF

*AC Parameters are guaranteed by DC correlated testing.

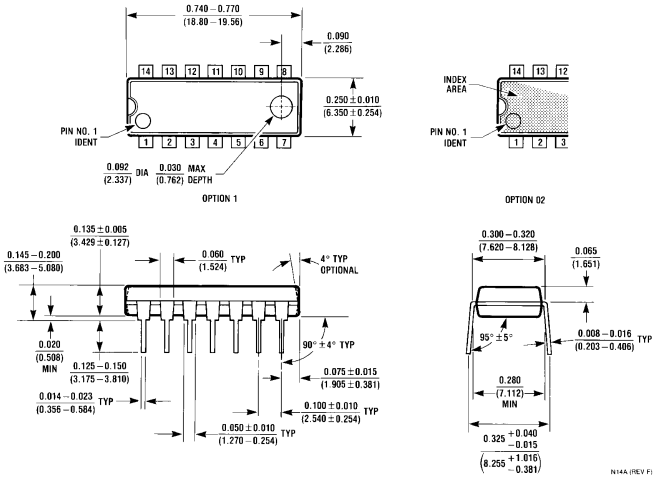
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note AN-90.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4023BMJ, CD4023BCJ, CD4025BMJ or CD4025BCJ
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4023BMN, CD4023BCN, CD4025BMN or CD4025BCN
NS Package Number N14A

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